Amendments to the Claims

This listing of claims will replace all prior versions, and listings of claims in the application.

Listing of Claims:

1 – 5. (cancelled)

6. (currently amended): ~~The~~ A semiconductor device ~~as claimed in claim 3,~~ comprising:

a substrate;

a mesh-shaped gate electrode located over a surface of the substrate, the mesh-shaped gate electrode having a plurality of openings aligned over respective source/drain regions of the substrate;

a gate dielectric layer interposed between the mesh-shape gate electrode and the surface of the substrate; and

at least one oxide region located in the substrate below the mesh-shaped gate electrode, wherein a thickness of the oxide region is greater than a thickness of the gate dielectric layer,

wherein the mesh-shaped gate electrode comprises a plurality of first elongate wirings extending parallel to one another, and a plurality of second elongate wirings extending parallel to one another, and wherein the first elongate wirings intersect the second elongate wirings to define an array of gate intersection regions over the surface of the substrate and to further define an array of source/drain regions of the substrate, and

wherein the at least one oxide region comprises a plurality of elongate oxide regions extending parallel to each other and lengthwise below the first elongate wirings of the mesh-shaped gate electrode.

7. (original): The semiconductor device as claimed in claim 6, wherein each of the plurality of elongate oxide regions have opposite ends which terminate at first and second elongate side oxide regions extending perpendicular to said plurality of elongate oxide regions.

8. (currently amended): ~~The~~ A semiconductor device ~~as claimed in claim 3,~~ comprising:

a substrate;

a mesh-shaped gate electrode located over a surface of the substrate, the mesh-shaped gate electrode having a plurality of openings aligned over respective source/drain regions of the substrate;

a gate dielectric layer interposed between the mesh-shape gate electrode and the surface of the substrate; and

at least one oxide region located in the substrate below the mesh-shaped gate electrode, wherein a thickness of the oxide region is greater than a thickness of the gate dielectric layer,

wherein the mesh-shaped gate electrode comprises a plurality of first elongate wirings extending parallel to one another, and a plurality of second elongate wirings extending parallel to one another, and wherein the first elongate wirings intersect the second elongate wirings to define an array of gate intersection regions over the surface of the substrate and to further define an array of source/drain regions of the substrate, and

said semiconductor device further comprising a common wiring located along at least one side of the array of source/drain regions, wherein each of the first and second elongate wirings are connected to the common wiring.

9. (original): The semiconductor device as claimed in claim 8, wherein the common wiring surrounds the array of source/drain regions.

10 – 11. (cancelled)

12. (currently amended): ~~The~~ A semiconductor device ~~as claimed in claim 3,~~ comprising:

a substrate;

a mesh-shaped gate electrode located over a surface of the substrate, the mesh-shaped gate electrode having a plurality of openings aligned over respective source/drain regions of the substrate;

a gate dielectric layer interposed between the mesh-shape gate electrode and the surface of the substrate; and

at least one oxide region located in the substrate below the mesh-shaped gate electrode, wherein a thickness of the oxide region is greater than a thickness of the gate dielectric layer,

wherein the mesh-shaped gate electrode comprises a plurality of first elongate wirings extending parallel to one another, and a plurality of second elongate wirings extending parallel to one another, and wherein the first elongate wirings intersect the second elongate wirings to define an array of gate intersection regions over the surface of the substrate and to further define an array of source/drain regions of the substrate, and

said semiconductor device further comprising:

a dielectric layer formed over the semiconductor substrate and the mesh-shaped gate electrode;

a plurality of elongate drain electrodes located over the dielectric layer and extending parallel to each other and diagonally over said array of source/drain regions;

a plurality of elongate source electrodes located over said dielectric layer and extending parallel to each other and diagonally over said array of source/drain regions;

wherein said source electrodes are electrically connected through said dielectric layer to source regions among said source/drain regions, and wherein said drain electrodes are electrically connected through said dielectric layer to drain regions among said array of source/drain regions, and wherein source electrodes and said drain electrodes are alternately arranged over said dielectric layer.

13. (original): The semiconductor device as claimed in claim 12, further comprising:

a common source electrode connected to said plurality of source electrodes; and

a common drain electrode connected to said plurality of drain electrodes.

14. (currently amended): ~~The~~ A semiconductor device ~~as claimed in claim 3,~~ comprising:

a substrate;

a mesh-shaped gate electrode located over a surface of the substrate, the mesh-shaped gate electrode having a plurality of openings aligned over respective source/drain regions of the substrate;

a gate dielectric layer interposed between the mesh-shape gate electrode and the surface of the substrate; and

at least one oxide region located in the substrate below the mesh-shaped gate electrode, wherein a thickness of the oxide region is greater than a thickness of the gate dielectric layer,

wherein the mesh-shaped gate electrode comprises a plurality of first elongate wirings extending parallel to one another, and a plurality of second elongate wirings extending parallel to one another, and wherein the first elongate wirings intersect the second elongate wirings to define an array of gate intersection regions over the surface of the substrate and to further define an array of source/drain regions of the substrate, and

said semiconductor device further comprising:

a first dielectric layer formed over the semiconductor substrate and the mesh-shaped gate electrode;

a plurality of elongate first electrodes located over said first dielectric layer and extending parallel to each other and diagonally over said array of source/drain regions;

a second dielectric layer formed over said first dielectric layer and said first electrodes;

a plurality of elongate second electrodes located over said second dielectric layer and extending parallel to each other and diagonally over said array of source/drain regions;

wherein said first electrodes are electrically connected through said first dielectric layer to either source or drain regions among said array of source/drain regions, and wherein said second electrodes are electrically connected through said first and second dielectric layers to the other of source or drain regions among said array of source/drain regions.

15. (original): The semiconductor device as claimed in claim 14, wherein said first electrodes and said second electrodes are alternately arranged over said substrate.

16. (original): The semiconductor device as claimed in claim 14, wherein said first electrodes and said second electrodes are arranged perpendicularly to each other over said substrate.

17. (original): The semiconductor device as claimed in claim 14, further comprising:

a common first electrode connected to said plurality of first electrodes; and

a common second electrode connected to said plurality of second electrodes.

18. (currently amended): ~~The~~ A semiconductor device ~~as claimed in claim 3,~~ comprising:

a substrate;

a mesh-shaped gate electrode located over a surface of the substrate, the mesh-shaped gate electrode having a plurality of openings aligned over respective source/drain regions of the substrate;

a gate dielectric layer interposed between the mesh-shape gate electrode and the surface of the substrate; and

at least one oxide region located in the substrate below the mesh-shaped gate electrode, wherein a thickness of the oxide region is greater than a thickness of the gate dielectric layer,

wherein the mesh-shaped gate electrode comprises a plurality of first elongate wirings extending parallel to one another, and a plurality of second elongate wirings extending parallel to one another, and wherein the first elongate wirings intersect the second elongate wirings to define an array of gate intersection regions over the surface of the substrate and to further define an array of source/drain regions of the substrate, and

said semiconductor device further comprising:

a first dielectric layer formed over the semiconductor substrate and the mesh-shaped gate electrode;

a first mesh-shaped electrode located over said dielectric layer, said first mesh-shaped electrode comprising a plurality of third elongate wirings extending parallel to one another and diagonally over said array of source/drain regions, and a plurality of fourth elongate wirings extending parallel to one another and diagonally over said array of source/drain regions, and wherein said third elongate wirings intersect said fourth elongate wirings;

a second dielectric layer formed over said first dielectric layer and said first mesh-shaped electrode;

a second mesh-shaped electrode located over said second dielectric layer, said second mesh-shaped electrode comprising a plurality of fifth elongate wirings extending parallel to one another and diagonally over said array of source/drain regions, and a plurality of sixth elongate wirings extending parallel to one another and diagonally over said array of source/drain regions, and wherein said fifth elongate wirings intersect said sixth elongate wirings;

wherein said first mesh-shaped electrode is electrically connected through said first dielectric layer to either source or drain regions among said array of source/drain regions, and wherein said second mesh-shaped electrode is electrically connected through said first and second dielectric layers to the other of source or drain regions among said array of source/drain regions.

19. (original): A semiconductor device comprising:

a substrate;

a mesh-shaped gate electrode located over a surface of the substrate, the mesh-shaped gate electrode having a plurality of openings aligned over respective source/drain regions of the substrate, and defining an array of gate intersection

regions over the surface of the substrate and an array of source/drain regions of the substrate;

a gate dielectric layer interposed between the mesh-shape gate electrode and the surface of the substrate; and

at least one oxide region located in the substrate below the intersection region of the gate electrode, wherein a thickness of the oxide region is greater than a thickness of the gate dielectric layer;

a dielectric layer formed over the semiconductor substrate and the mesh-shaped gate electrode;

a plurality of elongate first electrodes located over said dielectric layer and extending parallel to each other and diagonally over said array of source/drain regions;

a second dielectric layer formed over said first dielectric layer and said first electrodes;

a plurality of elongate second electrodes located over said dielectric layer and extending parallel to each other and diagonally over said array of source/drain regions;

wherein said first electrodes are electrically connected through said first dielectric layer to either source or drain regions among said array of source/drain regions, and wherein said second electrodes are electrically connected through said first and second dielectric layers to the other of source or drain regions among said array of source/drain regions.

20. (original): The semiconductor device as claimed in claim 19, wherein the at least one oxide region comprises an array of oxide regions located below the array of gate intersection regions, respectively.

21. (original): The semiconductor device as claimed in claim 19, wherein the at least one oxide region comprises a plurality of elongate oxide regions extending parallel to each other.

22. (original): The semiconductor device as claimed in claim 21, wherein each of the plurality of elongate oxide regions have opposite ends which terminate at first and second elongate side oxide regions extending perpendicular to said plurality of elongate oxide regions.

23. (original): The semiconductor device as claimed in claim 19, wherein said first electrodes and said second electrodes are alternately arranged over said substrate.

24. (original): The semiconductor device as claimed in claim 19, wherein said first electrodes and said second electrodes are arranged perpendicularly to each other over said substrate.

25. (original): The semiconductor device as claimed in claim 19, further comprising a common first electrode connected to said plurality of first electrodes, and a common second electrode connected to said plurality of second electrodes.

26. (original): The semiconductor device as claimed in claim 19, wherein the at least one oxide region is at least one field oxide region.

27. (previously presented): A semiconductor device comprising:
a substrate having an array of source/drain regions;

a mesh-shaped gate electrode located over a surface of the substrate, the mesh-shaped gate electrode having a plurality of openings aligned over respective ones of said array of source/drain regions of the substrate;

a gate dielectric layer interposed between the mesh-shape gate electrode and the surface of the substrate;

at least one oxide region located in the substrate below the mesh-shaped gate electrode, wherein a thickness of the oxide region is greater than a thickness of the gate dielectric layer;

a dielectric layer formed over the semiconductor substrate and the mesh-shaped gate electrode;

a plurality of elongate drain electrodes located over the dielectric layer and extending parallel to each other and diagonally over said array of source/drain regions; and

a plurality of elongate source electrodes located over said dielectric layer and extending parallel to each other and diagonally over said array of source/drain regions;

wherein source electrodes and said drain electrodes are alternately arranged over said dielectric layer, and

wherein each of the plurality of elongate drain electrodes terminate at one end at a first L-shaped common wiring, and each of the plurality of elongate source electrodes terminate at one end at a second L-shaped common wiring.

28. (original): The semiconductor device as claimed in claim 27, wherein the at least one oxide region comprises an array of oxide regions located below gate intersection regions of the mesh-shaped gate electrode, respectively.

29. (previously presented): A semiconductor device comprising:

a substrate having an array of source/drain regions;

a mesh-shaped gate electrode located over a surface of the substrate, the mesh-shaped gate electrode having a plurality of openings aligned over respective ones of said array of source/drain regions of the substrate;

a gate dielectric layer interposed between the mesh-shape gate electrode and the surface of the substrate;

at least one oxide region located in the substrate below the mesh-shaped gate electrode, wherein a thickness of the oxide region is greater than a thickness of the gate dielectric layer;

a dielectric layer formed over the semiconductor substrate and the mesh-shaped gate electrode;

a plurality of elongate drain electrodes located over the dielectric layer and extending parallel to each other and diagonally over said array of source/drain regions; and

a plurality of elongate source electrodes located over said dielectric layer and extending parallel to each other and diagonally over said array of source/drain regions;

wherein source electrodes and said drain electrodes are alternately arranged over said dielectric layer, and

wherein the at least one oxide region comprises a plurality of elongate oxide regions extending parallel to each other and lengthwise below elongate wirings of the mesh-shaped gate electrode.

30. (original): The semiconductor device as claimed in claim 29, wherein each of the plurality of elongate oxide regions have opposite ends which terminate at first and second elongate side oxide regions extending perpendicular to said plurality of elongate oxide regions.

31. (cancelled)

32. (original): The semiconductor device as claimed in claim 27, wherein the elongate drain electrodes and the elongate source electrodes are coplanar.

33. (original): The semiconductor device as claimed in claim 27, wherein the at least one oxide region is at least one field oxide region.

34. (original): A semiconductor device comprising:

a substrate;

a first mesh-shaped electrode located over a surface of the substrate;

a first dielectric layer interposed between the first mesh-shaped electrode and the surface of the substrate;

a second dielectric layer formed over the first mesh-shaped electrode;

a second mesh-shaped electrode located over said second dielectric layer;

a third dielectric layer formed over the second mesh-shaped electrode; and

a third mesh-shaped electrode located over said third dielectric layer.

35. (original): A semiconductor device as claimed in claim 34, wherein the first mesh-shaped electrode is gate electrode and the first dielectric layer is gate dielectric layer.

36. (original): A semiconductor device as claimed in claim 35, wherein the first mesh-shaped electrode includes a plurality of openings aligned over the substrate and defines an array of gate intersection regions over the substrate and an array of source/drain regions over the substrate.

37. (original): A semiconductor device as claimed in claim 36, further comprising at least one oxide region located in the substrate below the first mesh-

shaped electrode, wherein a thickness of the oxide region is greater than a thickness of the first dielectric layer.

38. (original): A semiconductor device as claimed in claim 37, wherein the oxide region is a field oxide region.

39. (original): A semiconductor device as claimed in claim 36, wherein the second mesh-shaped electrode is connected to one of the source/drain regions and the third mesh-shaped electrode is connected the other of the source/drain regions.